PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 143244.2 SB	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/IL 03/00125	International filing date *(day/month/year)* 18.02.2003	Priority date *(day/month/year)* 03.03.2002
International Patent Classification (IPC) or both national classification and IPC H01L27/06		
Applicant INTERON AS		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 8 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 15 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the opinion
   - II ☐ Priority
   - III ☒ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
24.09.2003	01.07.2004
Name and mailing address of the international preliminary examining authority: European Patent Office - P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Tx: 31 651 epo nl Fax: +31 70 340 - 3016	Authorized Officer Cabrita, A Telephone No. +31 70 340-2513

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/IL 03/00125

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:

Description, Pages

1, 2, 4-6, 8-15	as originally filed
2b	filed with the demand
2a, 2c, 2d, 3a, 7	filed with telefax on 24.03.2004
2e, 3	filed with telefax on 29.03.2004

Claims, Numbers

1-31	filed with telefax on 29.03.2004

Drawings, Sheets

1/8-8/8	as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).

   ☐ the language of publication of the international application (under Rule 48.3(b)).

   ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   ☐ contained in the international application in written form.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority in written form.

   ☐ furnished subsequently to this Authority in computer readable form.

   ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   ☐ the description, pages:

   ☐ the claims, Nos.:

   ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

III. Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

1. The questions whether the claimed invention appears to be novel, to involve an inventive step (to be non-obvious), or to be industrially applicable have not been examined in respect of:

   ☐ the entire international application,

   ☒ claims Nos. 4,5,20, 27-31

   because:

   ☐ the said international application, or the said claims Nos. relate to the following subject matter which does not require an international preliminary examination (specify):

   ☒ the description, claims or drawings *(indicate particular elements below)* or said claims Nos. 4,5,20 are so unclear that no meaningful opinion could be formed *(specify)*:

   see separate sheet

   ☐ the claims, or said claims Nos. are so inadequately supported by the description that no meaningful opinion could be formed.

   ☒ no international search report has been established for the said claims Nos. 27-31

2. A meaningful international preliminary examination cannot be carried out due to the failure of the nucleotide and/ or amino acid sequence listing to comply with the standard provided for in Annex C of the Administrative Instructions:

   ☐ the written form has not been furnished or does not comply with the Standard.

   ☐ the computer readable form has not been furnished or does not comply with the Standard.

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1,2,3,6-19,21-26
	No:	Claims	
Inventive step (IS)	Yes:	Claims	17,18
	No:	Claims	1,2,3,6-16,19,21-26
Industrial applicability (IA)	Yes:	Claims	1,2,3,6-19,21-26
	No:	Claims	

2. Citations and explanations

see separate sheet

Re Item III

Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

1. No examination can be made with respect to **claims 27-31** because no search has been performed regarding their subject-matter (Rule 66.1e PCT).

2. **Claims 4, 5** and **20** are formulated very broad and general wording without any clear technical features. Moreover, these claims appears to relate to the fabrication of a plurality of sensor chips on a wafer contrary to the subject-matter of claims 1 and 2 which relates to the fabrication of one sensor array. This renders the definition of the subject-matter so unclear that no meaningful opinion can be established with respect to these claims.

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Independent **claims 1, 2, 25** and **26** do not teach any clear and unambiguous structural relationship between all technical features of the sensor array, thereby rendering their subject-matter unclear in the sense of Article 6 PCT. It should be unambiguously clear on which side of the wafer the features are fabricated and how the individual features are electrically connected to each other. For instance, both in claims 1 and 2, it is not clear on which side of the wafer the electronics are provided. Moreover, in claim 2 for instance it is not clear to what feature the via is connected to.

For the assessment of inventive step below, independent claims 1, 2, 25 and 26 are interpreted with help of the description in the following way:

2. From the description (page 11 line 10-18) it is clear that **claims 1** and **25** refer to a sensor array comprising: an electronic processing circuit having sensor inputs and terminals formed on a first surface of a wafer, wherein the terminals are for connecting the processing circuit to external electronics for further processing; electrically conductive vias extending through the wafer from the sensor inputs to a second surface of the wafer opposite to the first surface; a sensor material deposited on the second surface, wherein the material is in contact with the electrically conductive vias through an ohmic contact.

3. From the description (page 12 line 5-9) it is clear that **claims 2** and **26** refer to a sensor

array comprising: an electronic processing circuit having sensor inputs on a first surface of the wafer, wherein a sensor material is deposited on the first surface and the material being in contact with the sensor inputs through an ohmic contact; electrically conductive vias extending through the wafer from the first surface to terminals disposed on the opposite second surface for connecting the processing circuit to external electronics for further processing.

4. The subject-matter of **claim 6** is not clear (Article 6 PCT) because of the use of the undefined feature "reverse side". It is not clear if this feature refers to the first or to the second surface. In the examination below both cases are considered.

5. The dependency of **claims 17** and **18** is not clearly defined. In the examination below it is assumed that claim 17 depends on 1 and claim 18 depends on 2.

6. The features of the device **claim 24** relate to a method of manufacturing such a device rather than clearly defining the device in terms of its technical features. The intended limitations are therefore not clear from this claim, contrary to the requirements of Article 6 PCT.

Reference is made to the following documents:

D1: US-A-4 104 674(HONEYWELL INC) 1 August 1978
D2: US-A-5 254 868 (SAITO YUTAKA) 19 October 1993
D3: US-A-5 998 292 (BURGHARTZ JOACHIM NORBERT ET AL) 7 December 1999

The subject-matter of **claims 1, 2, 3, 6-16, 19, 21-26** does not an involve inventive step in the sense of Article 33(3) PCT for the following reasons:

7. The document D1 discloses a sensor array and its method of manufacturing comprising the steps of (col.2 line 58-65; col.3 line 1-23): integrating electronic processing circuitry (fig.1b:24) on a first surface of a silicon wafer (fig.1b:10b), wherein sensor inputs are formed (fig.1b:26); forming electrically conductive vias through the wafer extending from the first surface to an opposite second surface (fig.1b: 20, 22, 26, 28), by using etching, ion implantation and thinning techniques; depositing sensor elements (fig. 1b:12; col.3 line 7-15, line 32-35) on the second surface opposite to the first surface, wherein electrodes

(fig.1b:20) are formed for connecting, through the conductive vias, the sensor elements to the sensor inputs of processing circuitry.

8. When comparing **claims 1, 6, 7, 12, 24** and **25** with D1, the remaining technical feature is that terminal nodes for external connection are formed on the first surface of the wafer. First of all, it is clear for the skilled person that a sensor array as disclosed in D1 should have terminals for external connection. Moreover, having the terminals on the side opposite to where the sensor elements are positioned is already known in the prior-art as is clearly described in D2. This document deals with a similar sensor array structure as the one in D1 and discloses on fig.11 an embodiment having the electronics and the external terminal on a side opposite to the one where the photoelements are disposed. Consequently, the skilled person would employ the teachings of D2 to a sensor array as described in D1 without any inventive skill. Claims 1, 6, 7, 12, 24 and 25 are therefore not inventive in the sense of Article 33(3) PCT.

9. Document D2 further discloses terminals in the form of metallized plates (figs.11 and 13). Consequently, for the same reason as discussed in item 8, the subject-matter of **claim 3** is not inventive (Article 33(3) PCT).

10. The method of manufacturing a sensor array **claim 2** and a sensor array **claim 26** refer to the case where the electronic processing circuit, the sensor inputs and the sensor elements are formed on the first surface of the wafer; and the electrically conductive vias extend through the wafer from the first surface to the terminal nodes disposed on the opposite second surface (see item 3).

Document D2 shows both alternatives, i.e. the sensor elements on the opposite surface of the sensor inputs and electronics (figs. 11 and 12(a)-(h)) or the sensor elements on the same surface as the sensor inputs and electronics (figs. 13 and 14(a)-(e)). Consequently, the skilled person would use one of those alternatives without inventive skill when the circumstances arise. Therefore, for the same reason as discussed under item 8, claims 2 and 26 are not inventive.

11. The subject-matter of **claim 8** referring to the use of a photomask cannot make the subject-matter inventive over the prior art. The use of lithographic techniques in the field of semiconductors technology is considered to be general common knowledge. Therefore, the skilled person would select this technique, in accordance with circumstances, without the exercise of inventive skill. Consequently, the subject-matter of claim 8 is not inventive in the sense of Article 33(3) PCT.

12. When comparing **claim 11** with D1, the remaining technical feature is the formation of the electrically conductive vias by using an etched via filled with electrically conductive material. This feature thus represents an alternative way of making an electrical via through a wafer. Such via structures are however very well known in the prior art as can be seen from document D3 (col.3 line 59-66; col.4 line 3-7, col 5 line 27-33), which describes a.o. the fabrication of interconnecting a CMOS wafer to a photodiode wafer (fig. 5 and col. 6 lines 55-67). Moreover document D1 explicitly mentions that other interconnect structures can be used (D1, col. 4 lines 8-14). Consequently, the skilled person would therefore regard it as a normal option to include this features in the manufacturing method of a sensor array described in document D1. Thus, the subject-matter of **claim 11** does not involve an inventive step in the sense of Article 33(3) PCT.

13. For the same reasons as in items 11 and 12, dependent **claims 9, 10** and **12-16** do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of inventive step.

14. Moreover, dependent **claims 19, 21-23** do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of inventive step.

each of which is fixed on a respective one of the signal takeout electrodes. A passivation film covers each signal takeout electrode where not in contact with its bump, and covering the clearances between the signal takeout electrodes. A base plate is provided with a plurality of contact pads corresponding to and in contact with the bumps.

US 5,254,868 (Yutaka) published October 19, 1993 and entitled "*Solidstate image sensor device*" discloses a semiconductor image sensor device comprising arrayed photo-sensors, wherein a connection electrode used for connecting an external circuit or an aperture on the connection electrode is provided at an opposite side surface to an illuminated surface, and a transparent substrate is provided above the arrayed photo-sensors. By such means the distance between a light source and the photo-sensors can be reduced so as to improve sensitivity and resolving power.

US 5,998,292 (Black *et al.*) issued Dec. 7, 1999 and entitled "*Method for making three dimensional circuit integration*" discloses a method for inter-connecting, through high-density micro-post wiring, multiple semiconductor wafers with lengths of about a millimeter or below. The method comprises etching at least one hole, defined by walls, at least partly through a semiconducting material; forming a layer of electrically insulating material to cover said walls; and forming an electrically conductive material on said walls within the channel of the hole.

JP 61 128564A2 (Fujitsu Ltd.) published Jun. 16, 1986 and entitled "*Semiconductor Device*" describes a process for forming a photodetecting section and a driving circuit on the surface and the back of the same substrate and connecting both by a wiring through a through-hole. An amplifier and other driving circuits are shaped to a Si growth layer, and an n type region is formed through the implantation of B+ ions in order to shape a P-N junction for a photodetecting element. Aluminum for a wiring is shaped so as to unit one part of the n type region and the Si growth layer side where the driving circuit is formed, and shaped through a method, such as ion beam evaporation, electron beam evaporation, etc. while masking sections except a required section. Aluminum is evaporated from

both upper and lower surfaces, and the wiring is connected by plating. A HgCdTe growth section in the photo-detecting element section and the Si growth layer are displaced, and formed on both surfaces of a sapphire substrate.

Such a configuration appears to relate to a single photo-detector only and the silicon is not pre-fabricated but rather is grown on top of the sapphire substrate.

EP1 045 450A2 (Agilent Technologies Inc.) published Oct. 18, 2003 and entitled "*Image sensor array device*" discloses an image sensor array that includes a substrate. An interconnect structure is formed adjacent to the substrate. An amorphous silicon electrode layer is adjacent to the interconnect structure. The amorphous silicon electrode layer includes electrode ion implantation regions between pixel electrode regions. The pixel electrode regions define cathodes of an array of image sensors. The electrode ion implantation regions provide physical isolation between the pixel electrode regions. The cathodes are electrically connected to the interconnect structure. An amorphous silicon I-layer is adjacent to the amorphous silicon electrode layer. The amorphous silicon I-layer forms an inner layer of each of the image sensors. A transparent electrode layer is formed adjacent to the image sensors. An inner surface of the transparent electrode layer is electrically connected to anodes of the image sensors and the interconnect structure. The amorphous silicon I-layer can further include I-layer ion implantation regions that provide physical isolation between the inner layers of the image sensors. The I-layer ion implantation regions align with the electrode ion implantation regions. An amorphous silicon P-layer can be formed adjacent to the amorphous silicon I-layer. The amorphous silicon P-layer forms an outer layer of each of the image sensors. The amorphous silicon P-layer can include P-layer ion implantation regions that provide physical isolation between the outer layers of the image sensors.

EP 537 514A2 (Mitsubishi corporation) published Apr. 21, 1993 and entitled "*Optoelectronic integrated circuit*" discloses an optoelectronic integrated circuit including a light receiving element for converting an optical signal to an electric signal and an electronic circuit for processing the electric signal. The light receiving element is disposed on a first main surface of the substrate and includes p

12, 1999. This article describes a multi-pixel CMOS array for visible light applications, such as photography. It employs thin film ASIC (TFA) technology to deposit an amorphous silicon detector on a pre-fabricated ASIC. The article does not address the need for a multi-pixel sensor array that is amenable to formation of a large area sensor assembly having multiple sensor arrays juxtaposed and makes no provision for such assembly.

None of the above cited references appears to relate to a multi-sensor detector where a silicon substrate is pre-fabricated to include all the sensor electronics and input connections; wherein a sensor layer is then grown on top of the pre-fabricated substrate and connects to the input connections therein by means of vias pre-formed in the substrate; and wherein terminal nodes for external connection of control signals etc. are formed on an opposite surface to the sensor layer thus avoiding dead space in the sensor material and permitting multiple sensor arrays to be juxtaposed so as to create large area sensors having substantially continuous sensitivity across the surface.

SUMMARY OF THE INVENTION

It is thus an object of the invention to provide an improved low-cost pixel sensor, which is amenable to closer packing, obviates the above-mentioned drawbacks that are contingent on the use of bump-bonding and the provision of I/O control-pads and allows multiple sensor modules to be juxtaposed so as to form a larger area sensor without requiring any further manufacturing process after assembly.

These objects are realized in accordance with a first embodiment of the invention by a method for fabricating a sensor array having a plurality of pixels, each pixel including an electronic processing circuit having a sensor input for coupling a sensor element to the electronic processing circuit, the sensor array further having a plurality of terminal nodes for external connection to respective electronic processing circuits of multiple pixels of power, I/O and control connections, the method comprising:

integrating the electronic processing circuits on a wafer so as to form an integrated circuit having at least one array of said electronic processing circuits with the sensor inputs and the terminal nodes being accessible from a first surface of the wafer;

in respect of each pixel, providing an electrically conductive via through the wafer extending from the respective sensor input to a second surface of the wafer opposite the first surface; and

depositing sensor material on the second surface of the wafer so that an unexposed surface thereof forms multiple electrodes each in registration with a corresponding one of the electrically conductive vias.

According to a variation of such a method there is provided a method for fabricating a sensor array having a plurality of pixels, each pixel including an electronic processing circuit having a sensor input for coupling a sensor element to the electronic processing circuit, the sensor array further having a plurality of terminal nodes for external connection to respective electronic processing circuits of multiple pixels of power, I/O and control connections, the method comprising:

integrating the electronic processing circuits on a wafer so as to form an integrated circuit having at least one array of said electronic processing circuits with the sensor inputs being accessible from a first surface of the wafer;

providing a plurality of electrically conductive vias through the wafer extending to a second surface of the wafer opposite the first surface, each of said electrically conductive vias being in registration with a respective terminal node in the sensor array; and

depositing sensor material on the first surface of the wafer so that an unexposed surface thereof forms multiple electrodes each in registration with the respective sensor input of a corresponding electronic processing circuit.

According to another aspect, the invention provides a multi-pixel sensor array comprising:

a wafer having integrated therein multiple electronic processing circuits each in respect of a respective pixel so as to form an integrated circuit having at least one

array of electronic processing circuits each electronic processing circuit having a respective sensor input, the sensor array further having a plurality of terminal nodes accessible from a first surface of the wafer for external connection to respective electronic processing circuits of multiple pixels of power, I/O and control connections,

in respect of each pixel, an electrically conductive via through the wafer extending from the respective sensor input to a second surface of the wafer opposite the first surface, and

a layer of sensor material deposited on the second surface of the wafer so as to form an array of sensor elements, so that an unexposed surface thereof forms multiple electrodes each in registration with a corresponding one of the electrically conductive vias.

According to yet another aspect, the invention provides a multi-pixel sensor array comprising:

a wafer having integrated therein multiple electronic processing circuits each in respect of a respective pixel so as to form an integrated circuit having at least one array of electronic processing circuits each electronic processing circuit having a respective sensor input accessible from a first surface of the wafer, the sensor array further having a plurality of terminal nodes for external connection to respective electronic processing circuits of multiple pixels of power, I/O and control connections,

in respect of each terminal node, an electrically conductive via through the wafer extending from the respective terminal node in the sensor array to a second surface of the wafer opposite the first surface, and

a layer of sensor material deposited on the first surface of the wafer so as to form an array of sensor elements, so that an opposite unexposed surface thereof forms multiple electrodes each in registration with the respective sensor input of a corresponding electronic processing circuit.

a layer of sensor material deposited on the first surface of the wafer so as to form an array of sensor elements, so that an exposed surface of the sensor material forms a first electrode that is common to all sensor elements towards which incident photons are directed, and an opposite unexposed surface thereof forms multiple second electrodes each in registration with the respective sensor input of a corresponding electronic processing circuit.

Referring to Fig. 7 there is shown a subsequent stage in the manufacturing process where desired amorphous or polycrystalline sensor material such as mercury iodide is grown on the top side of the wafer so as to form an array of sensor elements, each having an anode which is in ohmic contact with a respect one of the conductive vias 31 (shown in Fig. 6) and such that the opposite, exposed, surface of the sensor material forms a common cathode towards which incident photons are directed. Thus, Fig. 7 shows pictorially a composite wafer 35 having a lower silicon wafer 36 as described above, on top of which is grown an amorphous or polycrystalline sensor material 37 so as to form a matrix of sensor elements having a common cathode constituted by the upper surface of the device and a respective anode (not shown) that is effectively sandwiched between the upper sensor layer 37 and the lower silicon wafer 36 and is connected via a corresponding one of the vias formed in the silicon wafer 36.

As shown in Fig. 8, the wafer 35 is now scribed along the scribe lines so as to produce individual sensor chips 40, which in the specific example shown in the figure comprises 5 x 3 pixel elements in a two-layer structure having an upper layer 41 formed of a silicon wafer and having integrated therewith pixel electronics reference 23 in Fig. 4 and having a lower layer 42 on which the sensor elements themselves are deposited. Toward the upper layer 41 are also formed terminal nodes to allow for the external connection to the pixel electronics of power, I/O and control connections. This is typically done by means of terminal pads 43, which are metallized on the outer surface of the silicon wafer in known manner and formed already in an earlier stage of the fabrication corresponding to the silicon wafer 20 shown in Fig. 2. In use, access to an individual pixel in the sensor array is achieved by addressing the required pixel and the location of an active pixel in the sensor array is likewise determined by decoding its address. In a sensor array having, for example, 1024 pixels the required address bus has 10 lines and in general the required address bus for a pixel array having N pixels has $\log_2 N$ lines. Thus far fewer terminal nodes are required than sensor inputs.

CLAIMS:

1. A method for fabricating a sensor array having a plurality of pixels, each pixel including an electronic processing circuit having a sensor input (24) for coupling a sensor element to the electronic processing circuit, the sensor array further having a plurality of terminal nodes for external connection to respective electronic processing circuits of multiple pixels of power, I/O and control connections, the method comprising:

integrating the electronic processing circuits (25, 26) on a wafer (20) so as to form an integrated circuit having at least one array of said electronic processing circuits with the sensor inputs and the terminal nodes being accessible from a first surface of the wafer;

in respect of each pixel, providing an electrically conductive via (31) through the wafer (20) extending from the respective sensor input (24) to a second surface (28) of the wafer opposite the first surface;

depositing sensor material on the second surface of the wafer so that an unexposed surface thereof forms multiple electrodes each in registration with a corresponding one of the electrically conductive vias.

2. A method for fabricating a sensor array having a plurality of pixels, each pixel including an electronic processing circuit having a sensor input (24) for coupling a sensor element to the electronic processing circuit, the sensor array further having a plurality of terminal nodes for external connection to respective electronic processing circuits of multiple pixels of power, I/O and control connections, the method comprising:

integrating the electronic processing circuits (25, 26) on a wafer (20) so as to form an integrated circuit having at least one array of said electronic processing circuits with the sensor inputs being accessible from a first surface of the wafer;

providing a plurality of electrically conductive vias (31) through the wafer (20) extending to a second surface (28) of the wafer opposite the first surface, each

of said electrically conductive vias (31) being in registration with a respective terminal node in the sensor array; and

depositing sensor material on the first surface of the wafer so that an unexposed surface thereof forms multiple electrodes each in registration with the respective sensor input of a corresponding electronic processing circuit.

3. The method according to claim 1 or 2, further including:

forming on the second surface of the wafer a plurality of metallized terminal pads (43) each in ohmic contact with a respective one of the terminal nodes.

4. The method according to any one of Claims 1 to 3, wherein the integrated circuit includes multiple arrays of pixels and there is further included:

dividing the integrated circuit into discrete sensor arrays.

5. The method according to any one of Claims 1 to 4, further including:

assembling multiple sensor arrays edge to edge so as to form a composite sensor array having an extended surface area.

6. The method according to any one of Claims 1 to 5, further including:

thinning down the wafer (29) from a reverse side (28) thereof so as to remove the bulk of the wafer.

7. The method according to any one of Claims 1 to 5, wherein the wafer (20) is pre-thinned prior to providing the electrically conductive vias (31) through the wafer (20).

8. The method according to any one of Claims 1 to 7, wherein providing electrically conductive vias (31) through the wafer (20) includes:

coating the first surface of the wafer (20) with photomask (30) apart from exposed areas where the vias are to be formed; and

implanting the wafer with a material to which the photomask (30) is impervious, so that said material penetrates only the exposed areas and creates a local increase in the conductivity of the wafer to the second surface thereof, thus forming a matrix of conductive vias (31).

9. The method according to Claim 8, further including:

producing a complementary photomask that covers said area of the wafer on the second surface thereof and is in precise registration with the photomask (30) that is disposed on the first surface thereof.

10. The method according to Claim 8 or 9, wherein the wafer is based on silicon and said material is a p-type impurity.

11. The method according to any one of Claims 1 to 7, wherein providing electrically conductive vias (31) through the wafer (20) includes:

providing a photomask on the second surface only of the wafer so as to expose the wafer in direct registration with areas on the first surface of the wafer where the vias are to be formed;

partially etching holes through the wafer from the second surface toward the first surface so as to form partial bores; and

filling the bores with conductive material.

12. The method according to any one of Claims 1 to 7, wherein providing electrically conductive vias (31) through the wafer (20) includes:

partially etching holes through the wafer from the second surface so as to form partial bores;

implanting the wafer from the first surface thereof with a material to which the photomask (30) is impervious, so that said material renders the wafer conductive directly abutting each area where vias are to be formed; and

filling the partial bores with conductive material which abuts the wafer and completes the ohmic contact to the second surface of the wafer.

13. The method according to any one of Claims 1 to 7, wherein the electrically conductive vias (31) are formed in the wafer (20) prior to formation of the processing circuits by:

coating the first surface of the wafer (20) with photomask (30) for protecting an area surrounding an intended location of each via, whilst leaving said area exposed; and

implanting the wafer with a material to which the photomask (30) is impervious, so that said material penetrates only said area and creates a local increase in the conductivity of the wafer from the intended location of each via to the second surface thereof, thus forming a matrix of conductive vias (31) through the wafer (20).

14. The method according to any one of Claims 1 to 7, wherein the electrically conductive vias (31) are formed in the wafer (20) prior to formation of the processing circuits by:

coating the first surface of the wafer (20) with photomask (30) for protecting an area surrounding an intended location of each via, whilst leaving said area exposed, and

implanting the wafer with a material to which the photomask (30) is impervious, so that said material penetrates only said area and creates a local increase in the conductivity of the wafer from the intended location of each via through the wafer (20) to the second surface thereof, thus forming a matrix of conductive vias (31) through the wafer (20).

15. The method according to any one of Claims 1 to 7, wherein the electrically conductive vias (31) are formed in the wafer (20) prior to formation of the processing circuits by:

providing a photomask on the second surface only of the wafer so as to expose the wafer in direct registration with respective locations on the first surface of the wafer of intended vias,

etching holes through the wafer from the second surface to said locations (24), whilst not etching all the way through the wafer so as to form bores; and

filling the bores with conductive material.

16. The method according to any one of Claims 1 to 7, wherein the electrically conductive vias (31) are formed in the wafer (20) prior to formation of the processing electronics by:

partially etching holes through the wafer from the second surface so as to form partial bores;

implanting the wafer from the first surface thereof with a material to which the photomask (30) is impervious, so that said material penetrates only the intended via and renders the wafer conductive at an exposed area thereof; and

filling the partial bores with conductive material which abuts the wafer and completes the ohmic contact to the second surface of the wafer.

17. The method according to any one of Claims 1 to 16 when dependent on claim 1, wherein depositing the sensor elements includes:

growing amorphous or polycrystalline sensor material on the second surface of the wafer so as to form an array of sensor elements, each having an electrode having a first polarity which is in ohmic contact with a respective one of the conductive vias (31) and such that the exposed surface of the sensor material forms a common electrode having a polarity that is opposite to the first polarity.

18. The method according to any one of Claims 2 to 12 when dependent on claim 2, wherein depositing the sensor elements includes:

growing amorphous or polycrystalline sensor material on the first surface of the wafer so as to form an array of sensor elements, each having an electrode having a first polarity which is in ohmic contact with a respective one of the sensor inputs and such that the exposed surface of the sensor material forms a common electrode having a polarity that is opposite to the first polarity.

19. The method according to any one of Claims 13 to 18, wherein the sensor material and the terminal connections are formed on the wafer (20) prior to formation of the processing circuits (25, 26).

20. The method according to any one of Claims 1 to 19, wherein the integrated circuit includes multiple arrays of electronic processing circuits (25, 26) separated by scribe lines and there is further included:

scribing along the scribe lines so as to produce individual sensor chips (40).

21. The method according to any one of Claims 1 to 20, further including:

connecting terminal pads (43) metallized on an outer surface of the wafer via bump-bonds (45) to a ceramic board (46) that feeds bump-connections (47) through to surface mounted pins or bores; and

encapsulating so as to form a module (48).

22. The method according to Claim 21, further including:

mounting several of said modules (48) edge to edge so as to form a two-dimensional sensor (50) of larger surface area than a single module.

23. The method according to any one of the preceding claims, when used to fabricate a sensor array for a high energy photon imaging detector.

24. A sensor array or module manufactured according to any one of Claims 1 to 23.

25. A multi-pixel sensor array comprising:

a wafer having integrated therein multiple electronic processing circuits (25, 26) each in respect of a respective pixel so as to form an integrated circuit having at least one array of electronic processing circuits (25, 26) each electronic processing circuit having a respective sensor input (24), the sensor array further having a plurality of terminal nodes accessible from a first surface of the wafer for external connection to respective electronic processing circuits of multiple pixels of power, I/O and control connections,

in respect of each pixel, an electrically conductive via (31) through the wafer (20) extending from the respective sensor input (24) to a second surface (28) of the wafer opposite the first surface, and

a layer of sensor material deposited on the second surface of the wafer so as to form an array of sensor elements, so that an unexposed surface thereof forms multiple electrodes each in registration with a corresponding one of the electrically conductive vias (31).

26. A multi-pixel sensor array comprising:

a wafer having integrated therein multiple electronic processing circuits (25, 26) each in respect of a respective pixel so as to form an integrated circuit having at least one array of electronic processing circuits (25, 26) each electronic processing circuit having a respective sensor input (24) accessible from a first surface of the wafer, the sensor array further having a plurality of terminal nodes for external

connection to respective electronic processing circuits of multiple pixels of power, I/O and control connections,

in respect of each terminal node, an electrically conductive via (31) through the wafer (20) extending from the respective terminal node in the sensor array to a second surface (28) of the wafer opposite the first surface, and

a layer of sensor material deposited on the first surface of the wafer so as to form an array of sensor elements, so that an unexposed surface thereof forms multiple electrodes each in registration with the respective sensor input of a corresponding electronic processing circuit.

27. The sensor array according to Claim 25 or 26, being configured for use in a high energy photon imaging detector.

28. The sensor array according to any one of Claims 25 to 27, wherein the sensor material is amorphous or polycrystalline material that is grown on a surface of the wafer.

29. A sensor module (48) comprising an encapsulated sensor array according to any one of Claims 25 to 28 including:

terminal pads (43) metallized on an outer surface of the wafer via bump-bonds (45) to a ceramic board (46) that feeds bump-connections (47) through to surface mounted pins or bores.

30. A multi-module sensor assembly comprising a plurality of sensor modules according to Claim 29 mounted edge to edge so as to form a two-dimensional sensor (50) of larger surface area than a single module.

31. The sensor array according to any one of Claims 25 to 30, wherein an exposed surface of the sensor material forms a first electrode that is common to all sensor elements towards which incident photons are directed, and an opposite unexposed surface thereof forms multiple second electrodes each in registration with a corresponding one of the electrically conductive vias.